

FIG. 1 is a block diagram of a system 100 for processing multiple input signals. The system 100 includes a processor 170 and a plurality of parallel processing blocks 150. Each block 150 receives an input signal 160 and processes it through a series of delay elements 110 and multipliers 120 to produce a weighted signal. The weighted signals are then summed in a summation block 130. The outputs of the summation blocks 130 are combined in a final summation block 140 to produce the output signal y(k). The processor 170 is connected to the input signals 160 and the summation blocks 130, and it controls the weights w₁₁, w₁₂, ..., w_{1M}, w₂₁, w₂₂, ..., w_{2M}, ..., w_{N1}, w_{N2}, ..., w_{NM} applied in the multipliers 120.

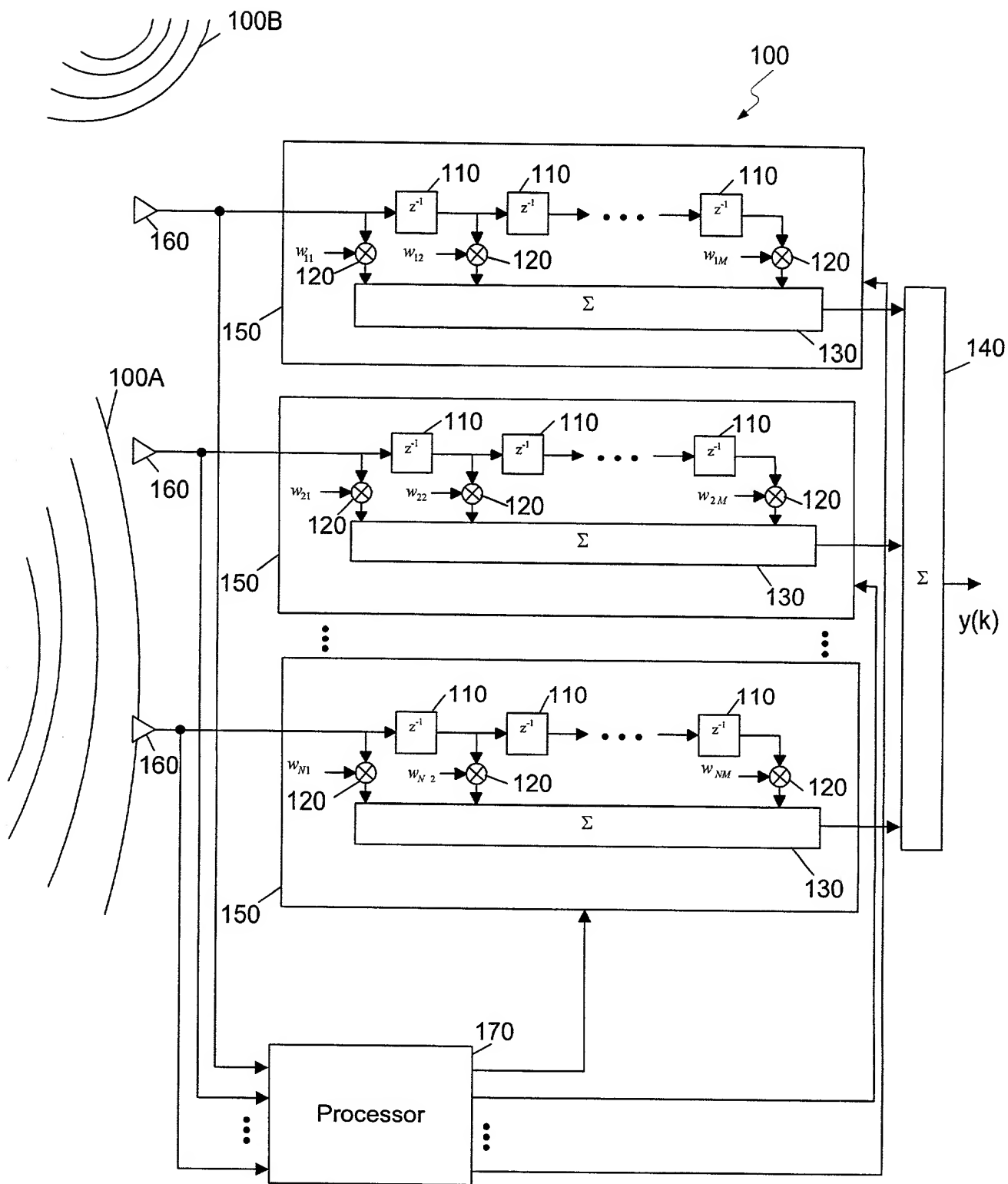


Fig. 1

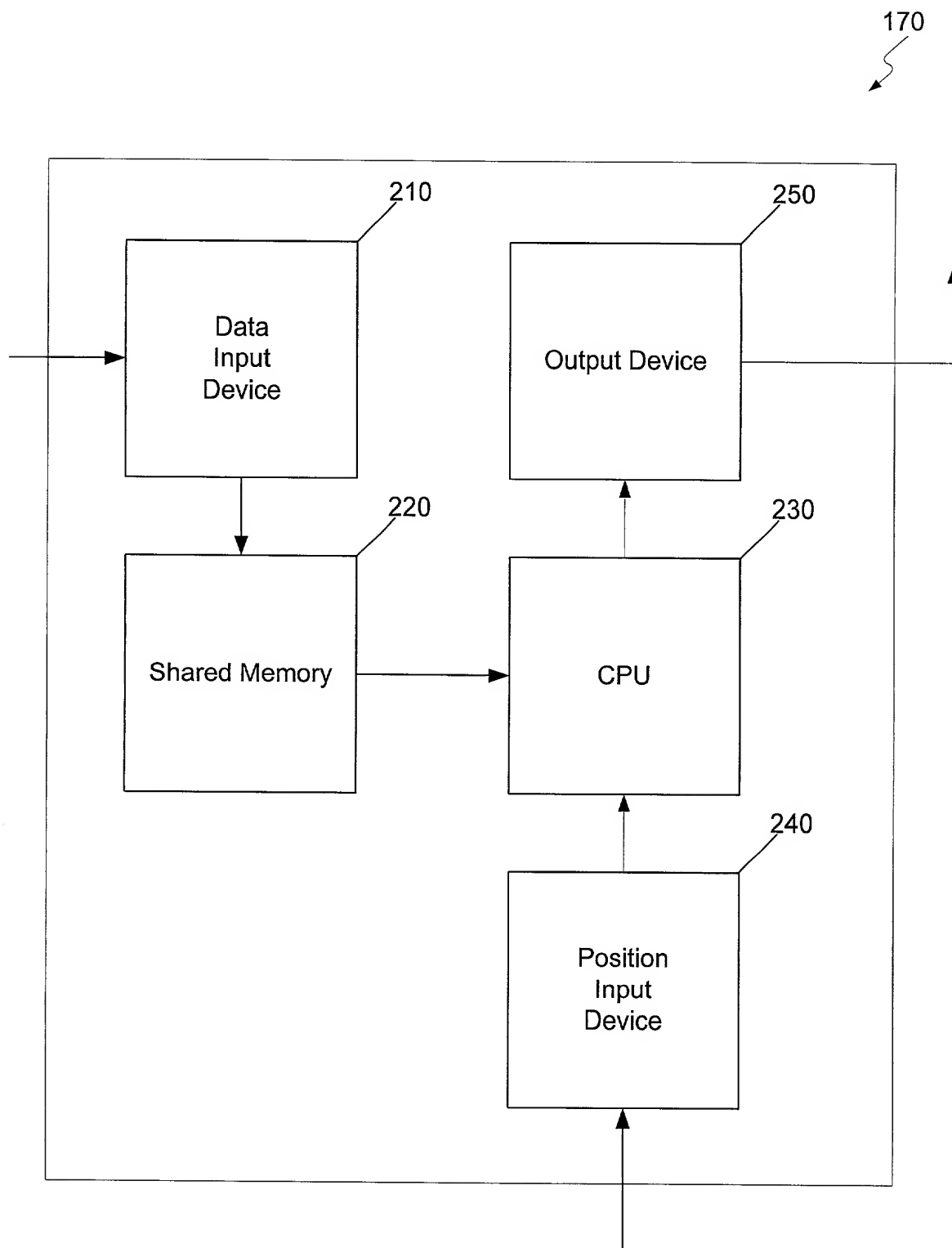


Fig. 2

FIG. 4 is a block diagram of a system 170. The system 170 includes an input device 210, a shared memory 220, a partial covariance processor 225, a CPU 230, an output device 250, and another input device 240. The input device 210 is connected to the shared memory 220 and the partial covariance processor 225. The shared memory 220 is connected to the partial covariance processor 225 and the CPU 230. The partial covariance processor 225 is connected to the CPU 230 and the output device 250. The CPU 230 is connected to the output device 250 and the input device 240. The input device 240 is connected to the CPU 230.

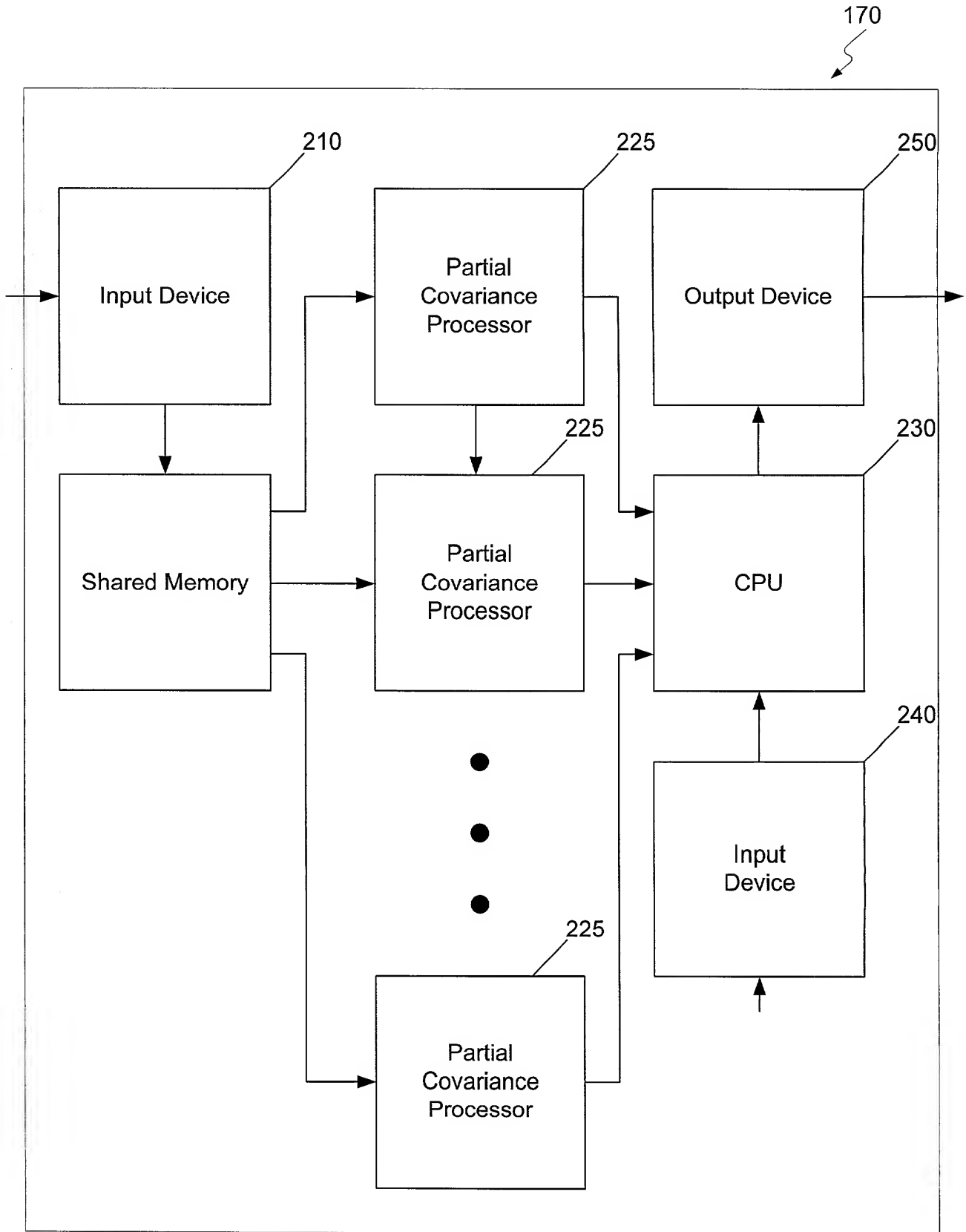


Fig. 4

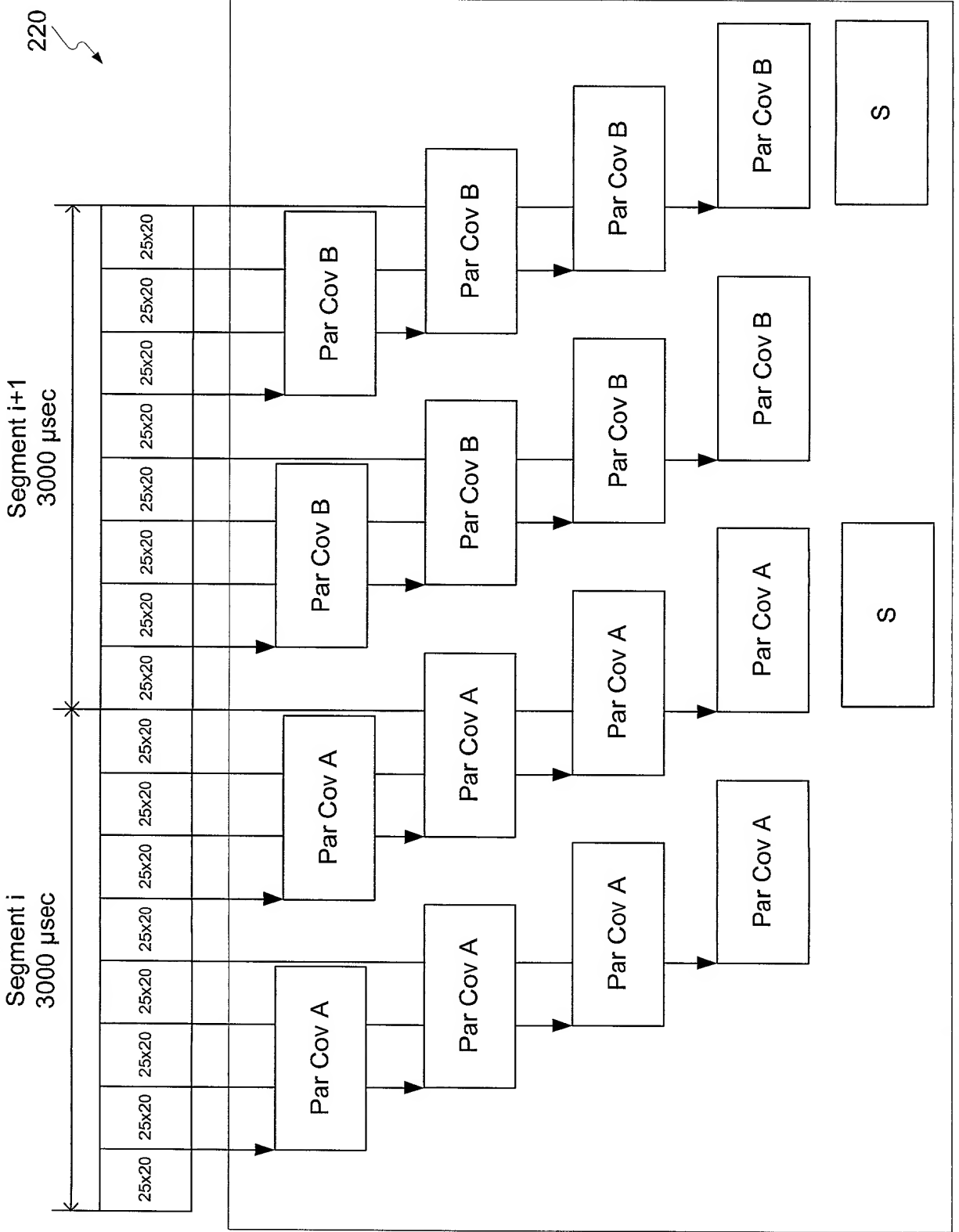


Fig. 5